Applicant's specification at page 4, lines 26-27 describes "A metal, such as tungsten or a tungsten alloy, is desirably used," as mentioned in Claims 4 and 18.

Applicant's specification at page 7, lines 24-26 describes "The structure of FIGs. 2(a)-2(e) thus is a three-dimensional semiconductor structure, having two levels of buried wiring lines; each level of buried wiring lines includes lines oriented in the x and the y planes," and at page 5, line 29 and page 6 lines 1-5 describes "In addition, deep trench capacitor 120 cuts through active layer 118, insulative material 116, and within substrate 110 between lines 114. The deep trench capacitor trench is filled with P+ silicon, and is surrounded by dielectric material 117. An alternative embodiment to that of FIG. 1(b) might have an additional level of buried elements, where the elements are located either in front of and/or behind the plane of the trench capacitor," as mentioned in Claims 8 and 15.

Applicant's specification at page 6, lines 26-29 and page 7, lines 1-2 describes "Referring first to FIG. 2(a), within N+ substrate 200 are two buried conductive layers, layer 204 and 206, each having a plurality of lines. Each layer is oriented in both the x and y planes; that is, each has a plurality of lines oriented in both the x and y planes. Insulative material 208 surrounds conductive layers 204 and 206. Active semiconductor layer 210 lies above the layer formed by insulative material 208," as mentioned in Claim 9.

Applicant's specification at page 5, lines 13-14 describes "Optionally, a connection between layers 102 and 104 may also be made, or between either layer and active semiconductor layer 108," and also at page 5, lines 23-25 describes "All the conductive layers provide for internal wiring within the semiconductor structure, to allow three-dimensional structures to be formed," as mentioned in Claims 12 and 20.

Applicant's specification at page 4, lines 3-5 describes "An alternative embodiment to that of FIG. 1(b) might have an additional level of buried elements, where the elements are located either in front of and/or behind the plane of the trench capacitor," as mentioned in Claim 15.

Applicant's specification at page 14, lines 28-29 and at page 15, lines 1-5 describes "In one embodiment, the devices are dynamic random-access-memories (DRAMs), including those available from Micron Technology, Inc., of Boise, Idaho. In other embodiments, the devices are static random-access-memories (SRAMs), flash memories, synchronous dynamic random-

access-memories (SDRAMs), extended-data-out random-access-memories (EDO RAMs), and burst-extended-data-out random-access-memories (BEDO RAMs), as those skilled in the art will appreciate," as mentioned in Claim 16.

Applicant's specification at page 4, lines 27-29 describes "Other metals include the non-radioactive elements selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and alloys of such elements," as mentioned in Claim 19.

Applicant's specification at page 5, lines 21-23 describes "These other layers may be positioned above or below the other layers, and may have lines oriented in a direction parallel to or orthogonal to the directions in which the lines of the other layers are oriented," as mentioned in Claim 21.

Drawings Objection

Applicant respectfully submits that the drawings do provide enablement commensurate with the scope of Claims 1-2, 4, 8-9, 11-12, 15-16, 19-21 for the following reasons and respectfully requests that the objection be withdrawn.

Applicant's specification at page 4, lines 15-25 describes "Within N+ substrate 100 (i.e., doped silicon) are two buried conductive layers, layer 102 and layer 104. Layer 102 includes a series of conductive lines separated by an insulative material, where the conductive lines are parallel to the view shown in FIG. 1(a), such that only one such line is seen. Layer 104 includes a series of conductive lines also separated by an insulative material, but where the conductive lines are perpendicular to the view shown in FIG. 1(a), such that two such lines are seen. Layer 102 may thus be described as oriented in an x plane, and layer 104 oriented in a y plane. A conductive element may refer to either a layer within a semiconductor structure, or a conductive line within such a layer," as mentioned in Claim 1 and shown in Figure 1(a).

Applicant's specification at page 13, lines 19-21 describes "The melting point of the metal or alloy used should desirably be sufficiently high to prevent its melting or other unwanted metallurgical changes during further processing of the silicon," as mentioned in Claims 2 and 11. That is, any conductive element in the drawings may include this feature, e.g., layers 112, 114.

Applicant's specification at page 4, lines 26-27 describes "A metal, such as tungsten or a tungsten alloy, is desirably used," as mentioned in Claims 4 and 18 and exemplified in the processing steps of Figures 2(a)-(g).

Applicant's specification at page 7, lines 24-26 describes "The structure of FIGs. 2(a)-2(e) thus is a three-dimensional semiconductor structure, having two levels of buried wiring lines; each level of buried wiring lines includes lines oriented in the x and the y planes," and at page 5, line 29 and page 6 lines 1-5 describes "In addition, deep trench capacitor 120 cuts through active layer 118, insulative material 116, and within substrate 110 between lines 114. The deep trench capacitor trench is filled with P+ silicon, and is surrounded by dielectric material 117. An alternative embodiment to that of FIG. 1(b) might have an additional level of buried elements, where the elements are located either in front of and/or behind the plane of the trench capacitor," as mentioned in Claims 8 and 15 and shown in Figures 2(a)-(e).

Applicant's specification at page 6, lines 26-29 and page 7, lines 1-2 describes "Referring first to FIG. 2(a), within N+ substrate 200 are two buried conductive layers, layer 204 and 206, each having a plurality of lines. Each layer is oriented in both the x and y planes; that is, each has a plurality of lines oriented in both the x and y planes. Insulative material 208 surrounds conductive layers 204 and 206. Active semiconductor layer 210 lies above the layer formed by insulative material 208," as mentioned in Claim 9 and shown in Figure 2(a).

Applicant's specification at page 5, lines 13-14 describes "Optionally, a connection between layers 102 and 104 may also be made, or between either layer and active semiconductor layer 108," and also at page 5, lines 23-25 describes "All the conductive layers provide for internal wiring within the semiconductor structure, to allow three-dimensional structures to be formed," as mentioned in Claims 12 and 20 and shown in Figure 2(a).

Applicant's specification at page 6, lines 3-5 describes "An alternative embodiment to that of FIG. 1(b) might have an additional level of buried elements, where the elements are located either in front of and/or behind the plane of the trench capacitor," as mentioned in Claim 15 and shown in Figure 1(b).

Applicant's specification at page 14, lines 28-29 and at page15 lines 1-5 describes "In one embodiment, the devices are dynamic random-access-memories (DRAMs), including those available from Micron Technology, Inc., of Boise, Idaho. In other embodiments, the devices are

static random-access-memories (SRAMs), flash memories, synchronous dynamic random-access-memories (SDRAMs), extended-data-out random-access-memories (EDO RAMs), and burst-extended-data-out random-access-memories (BEDO RAMs), as those skilled in the art will appreciate," as mentioned in Claim 16 and shown in Figure 4.

Applicant's specification at page 4, lines 27-29 describes "Other metals include the non-radioactive elements selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and alloys of such elements," as mentioned in Claim 19 and shown in Figure 1(a).
Applicant's specification at page 5, lines 21-23 describes "These other layers may be positioned above or below the other layers, and may have lines oriented in a direction parallel to or orthogonal to the directions in which the lines of the other layers are oriented," as mentioned in Claim 21 and shown in Figure 1(a) and Figure 2(a)-(b).

If any of these drawings do not satisfy the Examiner, Applicant will provide examples of drawings taken from issued U.S. patents to show that layers, e.g., layers 112, 114 of the present application, are sufficient to show structural elements that have specific features.

§112 Rejection of the Claims

Claims 1-21 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicant respectfully submits that the specification does provide enablement commensurate with the scope of Claims 1-2, 4, 8-9, 11-12, 15-16, 19-21 for the following reasons and respectfully requests that the objection be withdrawn.

Applicant's specification at page 4, lines 15-25 describes "Within N+ substrate 100 (i.e., doped silicon) are two buried conductive layers, layer 102 and layer 104. Layer 102 includes a series of conductive lines separated by an insulative material, where the conductive lines are parallel to the view shown in FIG. 1(a), such that only one such line is seen. Layer 104 includes a series of conductive lines also separated by an insulative material, but where the conductive lines are perpendicular to the view shown in FIG. 1(a), such that two such lines are seen. Layer 102 may thus be described as oriented in an x plane, and layer 104 oriented in a y plane. A

conductive element may refer to either a layer within a semiconductor structure, or a conductive line within such a layer," as mentioned in Claim 1. Further, not only does Figure 1(b) show and support a plurality of substantially parallel buried conductive elements, but so do Figures 1(a), 1(c), 2(a)-(c), (f), and (g), for example.

Applicant's specification at page 13, lines 19-21 describes "The melting point of the metal or alloy used should desirably be sufficiently high to prevent its melting or other unwanted metallurgical changes during further processing of the silicon," as mentioned in Claims 2 and 11.

Applicant's specification at page 4, lines 26-27 describes "A metal, such as tungsten or a tungsten alloy, is desirably used," as mentioned in Claims 4 and 18.

Applicant's specification at page 7, lines 24-26 describes "The structure of FIGs. 2(a)-2(e) thus is a three-dimensional semiconductor structure, having two levels of buried wiring lines; each level of buried wiring lines includes lines oriented in the x and the y planes," and at page 5, line 29 and page 6 lines 1-5 describes "In addition, deep trench capacitor 120 cuts through active layer 118, insulative material 116, and within substrate 110 between lines 114. The deep trench capacitor trench is filled with P+ silicon, and is surrounded by dielectric material 117. An alternative embodiment to that of FIG. 1(b) might have an additional level of buried elements, where the elements are located either in front of and/or behind the plane of the trench capacitor," as mentioned in Claims 8 and 15.

Applicant's specification at page 6, lines 26-29 and page 7, lines 1-2 describes "Referring first to FIG. 2(a), within N+ substrate 200 are two buried conductive layers, layer 204 and 206, each having a plurality of lines. Each layer is oriented in both the x and y planes; that is, each has a plurality of lines oriented in both the x and y planes. Insulative material 208 surrounds conductive layers 204 and 206. Active semiconductor layer 210 lies above the layer formed by insulative material 208," as mentioned in Claim 9.

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Applicant's specification at page 14, lines 28-29 and at page15 lines 1-5 describes "In one embodiment, the devices are dynamic random-access-memories (DRAMs), including those available from Micron Technology, Inc., of Boise, Idaho. In other embodiments, the devices are static random-access-memories (SRAMs), flash memories, synchronous dynamic random-access-memories (SDRAMs), extended-data-out random-access-memories (EDO RAMs), and burst-extended-data-out random-access-memories (BEDO RAMs), as those skilled in the art will appreciate," as mentioned in Claim 16.

Applicant's specification at page 4, lines 27-29 describes "Other metals include the non-radioactive elements selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and alloys of such elements," as mentioned in Claim 19.

Applicant's specification at page 5, lines 21-23 describes "These other layers may be positioned above or below the other layers, and may have lines oriented in a direction parallel to or orthogonal to the directions in which the lines of the other layers are oriented," as mentioned in Claim 21.

§103 Rejection of the Claims

Claims 1-21 were rejected under 35 USC § 103(a) as being unpatentable over Okumura (U.S. Patent No. 4,912,535). Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found in Okumura (U.S. Patent No. 4, 912, 535). Since all the elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

The Office Action admitted that Okumura does not teach substantially parallel buried conductive elements. But, the Office Action maintained that this is inherent in Okumura for the reasons set forth on pages 7-8 of the Office Action. Applicant respectfully disagrees because the Office Action has not established a *prima facie* case of inherency because, as recited in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art," citing Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The Office Action does not even assert that the allegedly inherent characteristic is necessary. To serve as an anticipation when a reference is silent about the asserted inherent characteristic, the gap in the reference may be filled with recourse to extrinsic evidence. But, such evidence must make clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). Applicant respectfully submits that the Examiner has not produced extrinsic evidence to show that substantially parallel buried conductive elements recited in claim 1 is necessarily present in Okimura.

Applicant requests reconsideration and allowance of independent claims 1, 8, and 15 along with their respective dependent claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 5 Jan '05

By _____
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Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5 day of January, 2005.

Tina Kowal

Name

Signature